



Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
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	Applicant:	
	Mostafazadeh et al.	
Filing Date	Group	
08/27/2003	2811	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
* <i>N</i>	A	6,677,235	1/13/04	Yegnashankaran, et al.	438	667	12/3/2001
* <i>P</i>	B	6,607,941	12/19/03	Prabhu, et al.	438	113	1/11/2002
* <i>P</i>	C	6,498,381	12/24/02	Halahan, et al.	257	449	2/22/2001
* <i>P</i>	D	6,322,903	11/27/01	Siniaguine, et al.	428	617	12/6/1999

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
<i>N</i>	E	Reche, John, "Wafer Thinning and Thru-Silicon Vias: The Path to Wafer Level Packaging", Tru-Si Technologies, IEEE/CPMT Meeting, Santa Clara, CA, May 10, 2000, 42 Pages.
<i>N</i>	F	Tru-Si Technologies, "Thru Silicon Interconnects", 33 Pages.
<i>N</i>	G	Advanced Semiconductor Engineering Korea, Inc., "CMOS Image Sensor", http://www.asekr.com/doc/ASE_korea_Image_Sensor_overview.pdf , pages 4 and 5.
Examiner <i>Nitin Parulkar</i>		Date Considered <i>08-21-04</i>

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.